DETAILED ACTION

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Transmit NOP (19 in the drawings).

The drawings are also objected to because there are no descriptive labels on parts of Figures 2 and 3. Important parts of the invention, such as the inputs, outputs, the memory banks, the DRAM module, the command scheduler, the memory bank control unit, the command analyzer, the register file, and others should contain labels. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 3 is objected to because of the following informalities: improper grammar: "an command". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The phrase "may involve" renders the claim indefinite, since it is unclear what the claim is trying to encompass. The examiner suggests changing the entire phrase to "involves"; the claim has been so construed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 5, 10, 13, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Chauvel et al (US 6,412,048).

Regarding Claim 1, Chauvel teaches a method for communication between an IC (host 12) and an external DRAM (SDRAM 24), where the external DRAM has at least one memory bank (see description of how the memory is arranged into banks on Column 6 Lines 33-40) and communicates with the IC via two or more channels, wherein the transmission of memory bank commands is prioritized on the basis of a static priority allocation for commands (see the state machine of Figure 4, read/write in steps 49 and 64, deactivate in steps 54 and 68, and activate in steps 56 and 70 have specific and static places in the memory controller) and a dynamic priority allocation for channels (Column 15 Lines 19-24, also see Table 2 on Column 15 for a list of channels).

Regarding Claim 5, Chauvel teaches all limitations of Claim 1, wherein the dynamic priority allocation involves one of the channels losing the highest priority only when it can send a command (see Column 17 Lines 14-30, note that after a command has been sent the peripheral device gains priority over time and reverts back to normal priority when it can again send a command, also see Column 16 Lines 9-11, which indicates that each channel may not have multiple requests pending).

Regarding Claim 10, Chauvel teaches all limitations of Claim 1, wherein two successive access operations to a memory bank are permitted when they are made to

the same row in the memory bank (see Figure 4 and particularly steps 46 and 58, where if two successive requests are made to the same row in the memory bank they are permitted).

Claim 13 is the memory controller with the same limitations as Claim 1, and is rejected on the same grounds.

Claim 14 is the appliance for reading and/or writing to storage media with the same limitations of Claim 1, and is rejected on the same grounds.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chauvel in view of Kirsch (US 2004/0054844). Chauvel teaches all limitations of Claim 1 as described above. In addition, Chauvel teaches a Read or Write command having the highest priority, since neither an Activate nor a Precharge command is given unless a read or write is present (see Figure 4 in Chauvel). The Activate command is given next highest priority, since a Precharge command is only run if a new row in the bank must be activated. However, though Chauvel makes references to a burst terminate type

command (see STOP command on Table 1 and DMA_Burst_Req_size signal on Table 4), Chauvel does not say what kind of priority is given to such commands. Kirsch teaches a burst terminate command takes precedence over write and read commands (see how the burst terminate command resets the state machine to the active state in Figure 7, also see paragraph 0071 in Kirsch). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have implemented the burst terminate command as a higher priority command than read or write. This would be useful when a separate read or write request must be taken care of while the memory is in the middle of a lengthy burst (Chauvel mentions a scenario like this in Column 21 Lines 41-49, and though his solution is different, combining the two devices as described is another solution to the problem).

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chauvel in view of Jones et al (US 6,301,642). Regarding Claim 3, Chauvel teaches all limitations of Claim 1 as described above. However, he does not teach a channel being given the lowest priority after a command has been sent. Jones teaches a round robin style memory arbiter (Column 1 Lines 51-62 in Jones). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used this style for the channels instead of the way described by Chauvel, since in some embodiments each channel may have equal rights to access

the memory, and the round robin memory arbiter allows for fairer access than assigned priorities for each channel.

This combined device meets all limitations of Claim 4, since Chauvel meets all limitations of Claim 1, wherein the dynamic priority allocation involves one of the channels being given highest priority in the next clock cycle if it does not have the highest priority in the current clock cycle and another channel sends a command (see Column 1 Lines 51-62 in Jones, if the channel with highest priority sends a command a different channel will have highest priority on the next clock cycle, also see Column 16 Lines 9-11, which indicates that each channel may not have multiple requests pending).

Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chauvel in view of Wheeler et al (US 6,983,350). Regarding Claim 7, Chauvel teaches all limitations of Claim 1 as described above, as well as channels sharing the SDRAM resource (note Figure 4, where the next pending request, which could be from a different channel, is observed to see if it is on the same row, indicating joint use, also see Column 16 Lines 9-11 in Chauvel, which indicates that each channel may not have multiple requests pending). However, Chauvel does not teach giving no successive access operations to a jointly used memory bank. Wheeler teaches alternating memory banks such that no successive access operation accesses a jointly used memory bank (Column 5 Lines 33 to 42 in Wheeler). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to arrange memory operations in such a way. Wheeler provides the motivation

when he states that the bandwidth of the RAM is improved (Column 5 Lines 40-42 in Wheeler).

This combined device meets all limitations of Claim 9, since Chauvel meets all limitations of Claim 1, wherein two access operations to a memory bank always have an access operation to another memory bank effected between them (Column 5 Lines 33 to 42 in Wheeler, alternating between an even and odd memory bank places at least one access operation between each bank).

Claims 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chauvel in view of Chen et al (US 2003/0051108). Regarding Claim 8, Chauvel teaches all limitations of Claim 1 As described above. However, Chauvel does not teach a network provided which allows at least one channel to access various memory banks. Chen teaches a network (Bank Usage Sorter 110 in Chen) that allows the channels to access any memory bank (paragraph 0014, also see Figure 3 in Chen). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used this network to distribute the memory data evenly across the banks because this reduces costs (see Paragraph 0015 in Chen).

Note that this device meets all limitations of Claim 6, since the channels are accessing physically separate memory areas (banks WO – W7 in Chen) in the external DRAM.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chauvel in view of LaBerge (US 2001/0044885). Chauvel teaches all limitations of Claim 1 as described above. However, Chauvel is silent on the details of how the memory bank works. LaBerge teaches a memory bank that has a state machine (containing at least the states 'idle' and 'not idle', see Paragraph 0023 and Figure 8 in LaBerge). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used a state machine to control the memory banks because tracking idle states results in reducing latency incurred between successive memory operations (see Paragraph 0019 in LaBerge).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chauvel in view of the power point entitled "Random Access Memory". Chauvel teaches all limitations of Claim 1 as described above. However, Chauvel does not teach the composition of the DRAM memory. "Random Access Memory" teaches combining several RAM modules into a single RAM module and a chip enable signal (called chip select in the power point) to select the desired module (see Slides 17 and 18). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have combined the RAM modules this way because it allows for larger memories to be made (see Slide 18 in "Random Access Memory").

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark A. Giardino whose telephone number is (571) 270-3565. The examiner can normally be reached on M-R 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Robertson can be reached on (571) 272-4186. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M.G./

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2/22/2008

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